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Java based object oriented hardware specification and synthesis

Tommy Kuhn, Wolfgang Rosenstiel

January 2000 Proceedings of the 2000 conference on Asia South Pacific design automation

Full text available: pdf(428.53 KB) Additional Information: full citation, references, citings

An efficient ILP-based scheduling algorithm for control-dominated VHDL descriptions Michael Münch, Norbert Wehn, Manfred Glesner



October 1997 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 2 Issue 4

Full text available: pdf(375.99 KB) Additional Information: full citation, abstract, references, index terms

To adopt behavioral synthesis techniques in existing design flows, the synthesis methodology must provide the designer with a mechanism to specify a component's interface timing. This will permit pre- and postsynthesis validation through cosimulation with other subsystems or even through formal verification. In control-flow dominated designs, additional timing constraints will result in a complex specification/constraint system for which the scheduling problem has been shown to be NP-comple ...

Keywords: integer linear programming (ILP), scheduling, timing constraints

Behavioral network graph: unifying the domains of high-level and logic synthesis Reinaldo A. Bergamaschi

June 1999 Proceedings of the 36th ACM/IEEE conference on Design automation Full text available: pdf(787.07 KB) Additional Information: full citation, references, citings, index terms

An Efficient ILP-Based Scheduling Algorithm for Control-Dominated VHDL **Descriptions**

Authors: Michael Muench, Manfred Glesner, Norbert Wehn November 1996 Proceedings of the 9th International Symposium on System Synthesis

Full text available: pdf(940.81 KB)

Publisher Site

Additional Information: full citation, abstract

http://portal.acm.org/results.cfm?CFID=23928836&CFTOKEN=77648738&adv=1&COLL=...

In this paper, we present for the first time a mathematical framework for solving a special instance of the scheduling problem in control-flow dominated behavioral VHDL descriptions given that the timing of I/O signals has been completely or partially specified. It is based on a code-transformational approach which fully preserves the VHDL semantics. The scheduling problem is mapped onto an integer linear program (ILP) which can be constrained to be solvable in polynomial time, but still permits ...

Keywords: scheduling, control-flow dominated VHDL, ILP, time-constrainted scheduling, resource-constrained scheduling, code transformation

Analysis of different protocol description styles in VHDL for high-level synthesis
 M. Rahmouni, A. Jerraya, P. Kission, A. Mesquita, A. Pedroza, L. Pirmez
 September 1996 Proceedings of the conference on European design automation



Full text available: pdf(250.01 KB) Additional Information: full citation, references, index terms

From VHDL to efficient and first-time-right designs: a formal approach Peter F. A. Middelhoek, Sreeranga P. Rajan



April 1996 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 1 Issue 2

Full text available: pdf(722.99 KB)

Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index</u> <u>terms</u>

In this article we provide a practical transformational approach to the synthesis of correct synchronous digital hardware designs from high-level specifications. We do this while taking into account the complete life cycle of a design from early prototype to full custom implementation. Besides time-to-market, both flexibility with respect to target architecture and efficiency issues are addressed by the methodology. The utilization of user-selected behavior-preserving transformation steps e ...

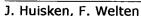
Keywords: CDFG, SFG, VHDL, correctness by construction, design methodology, rapid system prototyping, transformational design

Formulation and evaluation of scheduling techniques for control flow graphs
 Maher Rahmouni, Ahmed A. Jerraya
 December 1995 Proceedings of the conference on European design automation



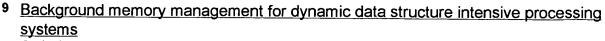
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FADIC: architectural synthesis applied in IC design





Full text available: pdf(197.94 KB) Additional Information: full citation, references, index terms





Gjalt de Jong, Bill Lin Carl Verdonck, Sven Wuytack, Francky Catthoor

December 1995 Proceedings of the 1995 IEEE/ACM international conference on

Computer-aided design

Full text available:



Additional Information: full citation, abstract, references, citings, index terms

Telecommunication network management applications often require application-specific ICs that use large dynamically allocated stored data structures. Currently available hardware synthesis environments typically do not support dynamic data structure concepts and their associated memory synthesis problems. In this paper we address the \fibackground memory management\fP task in a hardware design trajectory, which includes allocation of a distributed memory architecture, assignment and mapping of a ...

Keywords: Background memory management system level design telecommunication network applications

10 Efficient scheduling of conditional behaviors for high-level synthesis

Apostolos A. Kountouris, Christophe Wolinski

July 2002 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 7 Issue 3

Full text available: pdf(1.50 MB)

Additional Information: full citation, abstract, references, citings, index terms

As hardware designs get increasingly complex and time-to-market constraints get tighter there is strong motivation for high-level synthesis (HLS). HLS must efficiently handle both dataflow-dominated and controlflow-dominated designs as well as designs of a mixed nature. In the past efficient tools for the former type have been developed but so far HLS of conditional behaviors lags behind. To bridge this gap an efficient scheduling heuristic for conditional behaviors is presented. Our heuristic a ...

Keywords: Design automation, conditional behavior, high level synthesis (HLS), scheduling

11 An efficient multi-view design model for real-time interactive synthesis

Allen C.-H. Wu, Tedd S. Hadley, Daniel D. Gajski

November 1992 Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design

Full text available: pdf(502.62 KB) Additional Information: full citation, references, citings, index terms

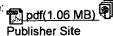
12 High level and system level synthesis: Hierarchical conditional dependency graphs as a unifying design representation in the CODESIS high-level synthesis system Apostolos A. Kountouris, Christophe Wolinski

September 2000 Proceedings of the 13th international symposium on System synthesis

Full text available: pdf(197.05 KB) Additional Information: full citation, abstract, references, citings

In high-level hardware synthesis (HLS) there is a gap on the quality of the synthesized results between data-flow and control-flow dominated behavioral descriptions. Heuristics destined for the former usually perform poorly on the latter. To close this gap, the CODESIS interactive HLS tool relies on a unifying intermediate design representation and adapted heuristics that are able to accommodate both types of designs as well as designs of a mixed data-flow and control-flow nature. Preliminary ex ...

13 Synthesis of low-power selectively-clocked systems from high-level specification L. Benini, P. Vuillod, G. de Micheli, Claudionor Coelho November 1996 Proceedings of the 9th International Symposium on System Synthesis Additional Information: full citation, abstract



In this paper we propose a technique for synthesizing low-power systems from a high-level specification. We analyze the control flow of the specification to detect mutually exclusive sections of the computation. A selectively-clocked interconnection of interacting FSMs is automatically generated and optimized where each FSM controls the execution of one section of computation. Only one of the interacting FSMs is active at any given clock cycle. while all the others are idle and their clock is st ...

Keywords: High level synthesis, low power, finite state machines, gated clocks.

14 Hardware/software partitioning of software binaries

Greg Stitt, Frank Vahid

November 2002 Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design

Full text available: pdf(290.80 KB)

Additional Information: full citation, abstract, references, citings, index terms

Partitioning an embedded system application among a microprocessor and custom hardware has been shown to improve the performance, power or energy of numerous examples. The advent of single-chip microprocessor/FPGA platforms makes such partitioning even more attractive. Previous partitioning approaches have partitioned sequential program source code, such as C or C++. We introduce a new approach that partitions at the software binary level. Although source code partitioning is preferable from a p ...

Keywords: FPGA, assembly language, binary translation, codesign, decompilation, hardware/software partitioning, low power, synthesis

15 Data and memory optimization techniques for embedded systems

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg

April 2001 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 6 Issue 2

Full text available: pdf(339.91 KB)

Additional Information: full citation, abstract, references, citings, index terms

We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transoformations. We next cover a broad spectrum of optimizati ...

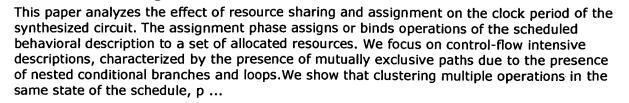
Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cache, data optimization, high-level synthesis, memory architecture customization, memory power dissipation, register file, size estimation, survey

16 Effects of resource sharing on circuit delay: an assignment algorithm for clock period optimization

Subhrajit Bhattacharya, Sujit Dey, Franc Breglez

April 1998 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 3 Issue 2

Full text available: pdf(260.26 KB) Additional Information: full citation, abstract, references, index terms



Keywords: clock period, high-level synthesis, resorce sharing

17 <u>High-level techniques for signal processing: System design for DSP applications in transaction level modeling paradigm</u>

Abhijit K. Deb, Axel Jantsch, Johnny Öberg

June 2004 Proceedings of the 41st annual conference on Design automation

Full text available: pdf(152.55 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we systematically define three **transaction level models** (TLMs), which reside at different levels of abstraction between the functional and the implementation model of a DSP system. We also show a unique language support to build the TLMs. Our results show that the abstract TLMs can be built and simulated much faster than the implementation model at the expense of a reasonable amount of simulation accuracy.

Keywords: DSP, grammar, system design, transaction level modeling

18 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 5 Issue 2

Full text available: pdf(385.22 KB)

Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index</u> terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survey ...

19 Register assignment through resource classification for ASIP microcode generation Clifford Liem, Trevor May, Pierre Paulin

November 1994 Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design

Full text available: pdf(653.28 KB)

Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index</u> terms

Application Specific Instruction-Set Processors (ASIPs) offer designers the ability for high-speed data and control processing with the added flexibility needed for late design specifications, accommodation of design errors, and product evolution. However, code generation for ASIPs is a complex problem and new techniques are needed for its success. The register assignment task can be a critical phase, since often in ASIPs, the number and functionality of available registers is limited, as t ...

A decade of reconfigurable computing: a visionary retrospective

R. Hartenstein

March 2001 Proceedings of the conference on Design, automation and test in Europe



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Print Format

3 A data flow graph exchange standard

van Eijndhoven, J.T.J.; Stok, L.;

Design Automation, 1992. Proceedings. [3rd] European Conference on , 16-19

March 1992

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Gupta, S.; Savoiu, N.; Dutt, N.; Gupta, R.; Nicolau, A.;

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[Abstract] [PDF Full-Text (960 KB)]

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[Abstract] [PDF Full-Text (1104 KB)]

6 An efficient ILP-based scheduling algorithm for control-dominated VHDL descriptions

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European Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings., 28 Feb.-3 March 1994 Pages:657

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[Abstract] [PDF Full-Text (328 KB)] IEEE CNF

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[Abstract] [PDF Full-Text (408 KB)] IEEE CNF

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which the VHDL specification is translated. This flowgraph mainly contains operations like
www.fzi.de/sim/publications/1995002-paper.pdf

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A Transformation for Integrating VHDL Behavioral Specificatio:n - With Synthesis And (Correct)
A Transformation for Integrating VHDL Behavioral Specificatio:n with Synthesis and Integrating VHDL Behavioral Specificatio:n with Synthesis and Software Generation Frank Vahid, Sanjiv wait statement are explained with the help of the flowgraph of Figure 3(a)The function current_time www.cs.ucr.edu/~vahid/pubs/eurodac94_transf.pdf

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